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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CARL A. ALBEROLA, AMIT R. GUPTA,
and TSUNG-HSIN LU

Appeal 2009-004177
Application 10/743,121
Technology Center 2100

Decided: February 23, 2010

Before JAMES D. THOMAS, ST. JOHN COURTENAY III,
and CAROLYN D. THOMAS, *Administrative Patent Judges*.

J. THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1, 2, 5-9, 11, 12, 14-17, and 21-24. Appellants have cancelled claims 3, 4, 10, 13, and 18-20. We have jurisdiction under 35 U.S.C. § 6(b).

We Affirm.

INVENTION

An instruction is pre-decoded at a direct memory access unit. (Abstract, Spec. 12, and Figs. 2, 3, 5, and 6.)

REPRESENTATIVE CLAIM

Below is reproduced independent claim 1:

1. A method, comprising:

retrieving a first instruction from a memory unit via an n-bit input path;

pre-decoding the first instruction at a direct memory access unit;

providing the pre-decoded first instruction from the direct memory access unit to a processing element via a q-bit output path, where $n < q$;

decoding the pre-decoded first instruction at the processing element;

executing the completely decoded instruction at the processing element;

determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed; and

arranging for a pre-decoded second instruction to not be provided from the direct memory access unit to the processing element.

PRIOR ART AND EXAMINER'S REJECTIONS

The Examiner relies on the following references as evidence of unpatentability:

Ramsdale	US 5,265,263	Nov. 23, 1993
Funderburk	US 5,291,525	Mar. 01, 1994
Dent	US 6.229,796 B1	May 08, 2001
Kessler	US 6,738,836 B1	May 18, 2004 (filed Aug. 31, 2000)
Kotani	US 6,789,140 B2	Sep. 07, 2004 (filed Aug. 08, 2002
Pechanek	US 6,848,041 B2	Jan. 25, 2005 (filed Apr. 28, 2003)

All claims on appeal stand rejected under 35 U.S.C. § 103. In a first stated rejection of claims 1, 2, 5-9, 11, and 14-17, the Examiner relies upon Kontani in view of Pechanek. In a second stated rejection of claim 12, the Examiner relies upon this initial combination of references, further in view of Kessler. Likewise, in a third stated rejection of claim 21, the Examiner relies upon the initial combination of references, further in view of Ramsdale. Next, in a rejection of dependent claims 22 and 23, the Examiner relies upon Kotani in view of Pechanek, further in view of Ramsdale and Funderburk. Lastly, in a fifth stated rejection of claim 24, the Examiner relies upon the combination of Kotani, Pechanek, Ramsdale, further in view of Dent.

Claim Grouping

Appellants present arguments as to independent claim 1 within the first stated rejection as representative of the subject matter of independent claims 1, 8, and 16. No dependent claims are argued within this first stated rejection. In a similar manner, the second through fifth stated rejections rely for patentability upon the arguments presented with respect to representative independent claim 1, including the separately stated rejection of independent claim 21.

ISSUE

Does the combination of Kotani and Pechanek teach the feature of representative independent claim 1 on appeal of a pre-decoded instruction having a "q-bit output path, where $n < q$"?

FINDINGS OF FACT (FF)

1. Appellants' Specification page 2, lines 16-20, teaches the state of the art:

> After an instruction is decoded, however, the processor might determine that the next sequential instruction should not be executed *(e.g.,* when the decoded instruction is associated with a jump or branch instruction). In this case, instructions that are currently in the decode and fetch stages may be removed from the pipeline. This situation, referred to as a "branch misprediction penalty," may reduce the performance of the processor.

(Spec. 2, ll. 16-20.)

2. With respect to the showing in the disclosed Figures 1 and 2, it is stated at Specification page 4, lines 14-16 that "[t]he pre-decoded instructions, however, would be significantly larger than the original instruction. For example, a 32-bit instruction might have one hundred bits after it is decoded." Likewise, with respect to the Figure 6 embodiment, it is stated at Specification page 5, lines 26-28 "that because the instruction has been pre-decoded, q may be larger than n (*e.g.*, because the pre-decoded instruction is larger than the original instruction)."

3. Kotani's Figure 9 shows a host CPU 210 to which is attached to a special processing unit 230 that includes a DMA controller 234. The operation of this special processing unit is shown in Figure 11 in flow chart form. Additionally, Kontani at page 11, lines 51-64 teach:

> In the above description, the interrupt was generated upon termination of the transfer. Alternatively, an interrupt may be generated on the following occasion, for example. That is, when preparing data in the main memory 20, the host CPU 210 may insert an interrupt instruction at a position immediately after certain data at which notification of completion of data transfer so far is necessary. The DMA controller 234 predecodes advanced instructions in drawing data, such as line drawing and filling-in of an area, while transferring the data to the drawing memory 240 or to the drawing section 232. Therefore, when the DMA controller 234 decodes an interrupt instruction, it can generate an interrupt for the host CPU 210 to notify the host CPU 210 of the progress of the transfer.

For emphasis here, this teaching indicates that the DMA controller 234 pre-decodes certain instructions although the pre-decoded function is not illustrated in Figure 9.

On the other hand, Figures 15 and 18 illustrate instruction prefetching as well as predecoding by respective precoders 437 in Figure 15 and 537 in Figure 18 at DMA controller 434/534. The drawing section 432 in Figure 15 and the corresponding drawing section 532 in Figure 18 appear to decode the resulting instructions. Kotani does not appear to indicate the relative instruction bit widths for instructions and predecoded instructions.

4. Pechanek teaches a scaleable instruction set architecture for hierarchical instructions sets utilizing dynamic compact instructions. The various portions of Figure 4 illustrate a compacted instruction that is in effect expanded to a 32 bit instruction as necessary. Corresponding predecode control functions occur in Figure 5 in element 512 and in element 812 in Figure 8.

PRINCIPLES OF LAW

> Section 103 forbids issuance of a patent when "the differences between the subject matte sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and discussed circumstances in which a patent might be determined to be obvious. *Id.* at 415 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on it precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 416. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 417.

The Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociate from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrated why some combinations would have been obvious where others would not." *Leapfrog Enters, Inc. v. Fisher-Prince Inc.,* 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. 398, 415 (2007)). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162 (citing *KSR*, 550 U.S. Ct. at 416-419).

ANALYSIS

We refer to, rely on, and adopt the Examiner's findings and legal conclusions set forth in the Answer. Our discussions will be limited to the following points of emphasis, which sufficiently expand upon the teachings of the relied upon prior art. To the extent Appellants' arguments beginning at page 6 of the Brief argue the absence of execution of certain instructions in the last clauses of representative independent claim 1 on appeal, finding of fact 1 indicates that such was known in the art anyway for certain known types of instructions.

The focus of Appellants' arguments, however, appears to be directed to the feature of representative independent claim 1 on appeal providing a pre-decoded instruction output path of q-bits that are greater than the n-bit path of the instruction itself before predecoding it. This is reflected in finding of fact 2 according to Appellants' disclosed invention as well as by the symbolic representation in representative independent claim 1 on appeal of n being less than q, which may be logically restated as q greater than n.

The Examiner relied upon the showing in Figure 9 and the teaching at column 11 we reproduced in finding of fact 3 of Kotani as illustrating that predecoding within a DMA unit or at a DMA unit is representative of the teachings associated with this Figure. Apparently, what has not been appreciated by the Examiner and Appellants are the actual teachings and the illustrations of a predecoding function in a corresponding manner in the illustrated embodiments shown in Figures 15 and 18 of Kotani.

The Examiner has recognized, as we have noted in finding of fact 3, that Kotani does not appear to teach the relative bit widths of the respective paths for instructions and in their predecoded versions. Since Kotani is essentially silent as to this feature, the Examiner properly turns to Pechanek for associated teachings that we have noted in finding of fact 4. We observe that Appellants' arguments in the Brief do not actually contest the teachings the Examiner has relied upon in Pechanek as to this feature. We conclude that it would have been obvious for the artisan to have utilized the teachings of Pechanek to enhance or obviate the noted deficiencies in Kotani as to this feature. To increase clock speed, as recognized by the Examiner's rationale, is consistent with the aim of Kotani's inventive disclosure.

To the extent Appellants' arguments challenge the proper combinability of these references at pages 8 and 9 of the Brief, our citation of the above-noted case law argues otherwise. Moreover, the Examiner has addressed this argument at pages 13-15 of the Answer by directly relying upon the United States Supreme Court's decision in *KSR* we noted earlier. The Examiner properly notes that more expansive rationales than a teaching-suggestion-motivation line of reasoning are permitted by this case law, including combining prior art elements according to known methods to yield predictable results. No Rely Brief has been filed by Appellants to contest the Examiner's responsive arguments in the Answer.

CONCLUSON AND DECISION

The combination of teachings of Kotani and Pechanek are proper within 35 U.S.C. § 103 and indicate that it was known in the art that a predecoded instruction may have a bit width greater than the initial instruction itself, as reflected in representative independent claim 1 on appeal. Based upon Appellants' grouping of the claims, all claims on appeal, claims 1, 2, 5-9, 11, 12, 14-17, and 21-24, are unpatentable over the cited prior art of record.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

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